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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,365	10/07/2003	Ryota Nishikawa	60188-662	3864

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2835	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PN

Office Action Summary	Application No.	Applicant(s)	
	10/679,365	NISHIKAWA ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/07/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 2 is objected to because of the limitation "stepped down from the predetermined voltage in order". It is unclear as to what order applicant is claiming. Appropriate correction is required.

Claims 14 and 31 are objected to because of the following informalities: line 2 "the regions is further divided" should be changed to read, "the regions are further divided".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al. (U.S. Pat. No. 5,610,449)

With respect to claims 1 and 20 Takahashi teaches an integrated circuit device, comprising a circuit block including a plurality of components (see components

distributed in Fig. 1), wherein at least one of the plurality of components is supplied with a voltage having a value different from that supplied to the other component or components. See also Fig. 1 some components receive 12v others receive 5v for example

With respect to claim 8 Takahashi teaches the plurality of components are divided and placed in a plurality of regions corresponding to the values of voltages to be supplied to the respective regions (see Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (U.S. Pat. No. 5,610,449) in view of Shimada (U.S. Pat. No 5,631,502).

With respect to claim 2 Takahashi teaches including a plurality of power circuits for respectively supplying voltages (column 1 lines 54-56) having mutually different values to the circuit block, wherein one of the power supplies is for supplying a predetermined voltage and the other power supplies are for respectively supplying voltages stepped down ("chopped down" column 2 lines 55-60) from the predetermined voltage in order. While it is held by the examiner the power circuits of Takahashi meet

the power supply limitation, if it is held by applicant otherwise It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Takahashi to include use of multiple supplies as seen in Shimada (Fig. 1 and 8).

Claims 3, 4-7, 9-13, 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsushi (JP 08181215) in view of Takahashi et al. (U.S. Pat. No. 5,610,449)

All references hereinafter to Katsushi refer to a machine translation attached to this office action.

With respect to claim 3 Katsushi teaches a Semiconductor device with multiple supply wiring and a signal delay means (see paragraph 0016) to send a signal to the functional block under certain conditions. Katsushi does not teach a circuit block including a plurality of components wherein at least one of the pluralities of components is supplied with a voltage having a value different from that supplied to the other component or components. Katsushi merely goes so far to show contacts for components to be connected (item 5 fig 6). Takahashi teaches an integrated circuit device, comprising a circuit block including a plurality of components (see components distributed in Fig. 1), wherein at least one of the plurality of components is supplied with a voltage having a value different from that supplied to the other component or components. See also Fig. 1 some components receive 12v others receive 5v for example. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Katsushi to mount a plurality of components similar to those seen in Takahashi in order to supply differing voltages to a plurality of components.

With respect to claim 4 Katsushi as modified by Takahashi teaches at least one of the plurality of components which belongs to a path having a signal delay value. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the largest signal delay value to be less than or equal to an admissible maximum signal delay value in order for the device to safely function.

With respect to claim 5 Katsushi as modified by Takahashi teaches at least one of the plurality of components belonging to a path other than the path having the largest signal delay value is supplied with a voltage lower than the voltage supplied to the path having the largest signal delay value.

With respect to claims 6, 12, 23 and 26 Katsushi as modified by Takahashi teaches at least two of the plurality of components belonging to an identical path (see fig. 6 in Katsushi wherein multiple terminals in the same region) are supplied with voltages having at least two values, based on the signal delay value.

With respect to claims 7 and 24 Katsushi as modified by Takahashi teaches if step-down ("chopped down" column 2 lines 55-60 Takahashi) of a voltage to be supplied to part of the components belonging to a first path is admitted based on the signal delay value which is characteristic of the path, at least one of the components belonging to both of the first path and a second path is supplied with a voltage lower than a voltage supplied to the other component or components belonging to the first path.

With respect to claim 9 Takahashi teaches including a plurality of power circuits for respectively supplying voltages (column 1 lines 54-56) having mutually different

values to the circuit block, wherein one of the power supplies is for supplying a predetermined voltage and the other power supplies are for respectively supplying voltages stepped down ("chopped down" column 2 lines 55-60) from the predetermined voltage in order. While it is held by the examiner the power circuits of Takahashi meet the power supply limitation, if it is held by applicant otherwise It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Katsushi to include the components and voltage conversion components in order to supply multiple voltages.

With respect to claims 10 and 27 Katsushi teaches at least one of a plurality of power lines connected to the respective ones of the plurality of components is separated so that the regions (see layers of figure 6) corresponding to the values of the voltages to be supplied to the components are defined.

With respect to claims 11 and 30 Katsushi is silent on placement of the plurality of components however does show contacts in Fig. 6 placed in regions. Takahashi teaches a plurality of components is placed in one of the regions (see regions shown in dashed lines on Fig. 1). Katsushi teaches the signal delay value in the transmission. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the components in regions in accordance with the signal delay as components requiring similar voltages may be grouped together in circuitry.

With respect to claim 13 and 29 Katsushi as modified by Takahashi teaches if step-down ("chopped down" column 2 lines 55-60 Takahashi) of a voltage to be supplied to part of the components. Katsushi teaches a first path is admitted based on

the signal delay (paragraph 0016) value caused under a give condition along a path to which each of the plurality of components belong, at least one of the components belonging to both of the first path and a second path is placed in a region supplied with a voltage lower (see at least voltage vales 3.3 and 2.5 in Fig. 6) than a voltage supplied to a region in which the other component or components belonging to the first path is placed.

With respect to claim 21-22 and 25 Katsushi teaches signal delay considerations under given conditions. Katsushi is silent on the use of statistical calculations in the path delay because the discussion of statistical calculations is meaningless in when referring to a single device and takes on meaning when discussing multiple devices. It would have been obvious to one of ordinary skill in the art at the time of the invention to use statistical computations to determine a signal delay and assure it is within a maximum signal delay value to insure the production of quality devices.

Claims 14-19 and 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsushi (JP 08181215) in view of Takahashi et al. (U.S. Pat. No. 5,610,449) as applied to claim 8 above, and further in view of Barber et al. (U.S. Pat. No 6,600,220)

With respect to claims 14 and 31 Katsushi as modified by Takahashi teaches regions with multiple components, which receive power and spacing the components from the power line. Neither Katsushi nor Takahashi clearly teach further dividing a region. Barber teaches a multi-region chip (Fig. 7) which is then further divided into smaller regions such as region 80A a power supply regions in order to protect other

regions from noise. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Katsushi as modified by Takahashi to further divide a region to reduce noise.

With respect to claims 15 and 32 while the spacing relative to an IR-drop is not specifically disclosed it would have been obvious to divide the regions of Barber to take in account the IR-drop, heat or other noise considerations.

With respect to claims 16 and 33 Barber teaches regions are further divide to reduce noise. Takahashi as modified by Katsushi teach placing components in the further-divided regions, in accordance with a signal delay value caused under a given condition along a path to which said each of the components belongs.

With respect to claim 17 Katsushi as modified by Takahashi teaches at least one of the plurality of components which belongs to a path having a signal delay value. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the largest signal delay value to be less than or equal to an admissible maximum signal delay value in order for the device to safely function.

With respect to claims 18 and 34 Barber teaches a multi-region chip (Fig. 7) which is then further divided into smaller regions such as region 80A a power supply regions in order to protect other regions from noise. Katsushi as modified by Takahashi teaches at least one of the plurality of components belonging to a path other than the path having the largest signal delay value is supplied with a voltage lower than the voltage supplied to the path having the largest signal delay value. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the largest

signal delay value to be less than or equal to an admissible maximum signal delay value in order for the device to safely function.

With respect to claims 19 and 35 Barber teaches the circuit is divided into a plurality of regions in accordance with the number of connection elements connected to the power line as the spacing of regions within the IC chip is obvious to suit the space requirements of the components mounted thereon.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn D. Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

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